SYSC3601
Microprocessor Systems

Unit 4:
8086/88 Hardware & Bus Structure

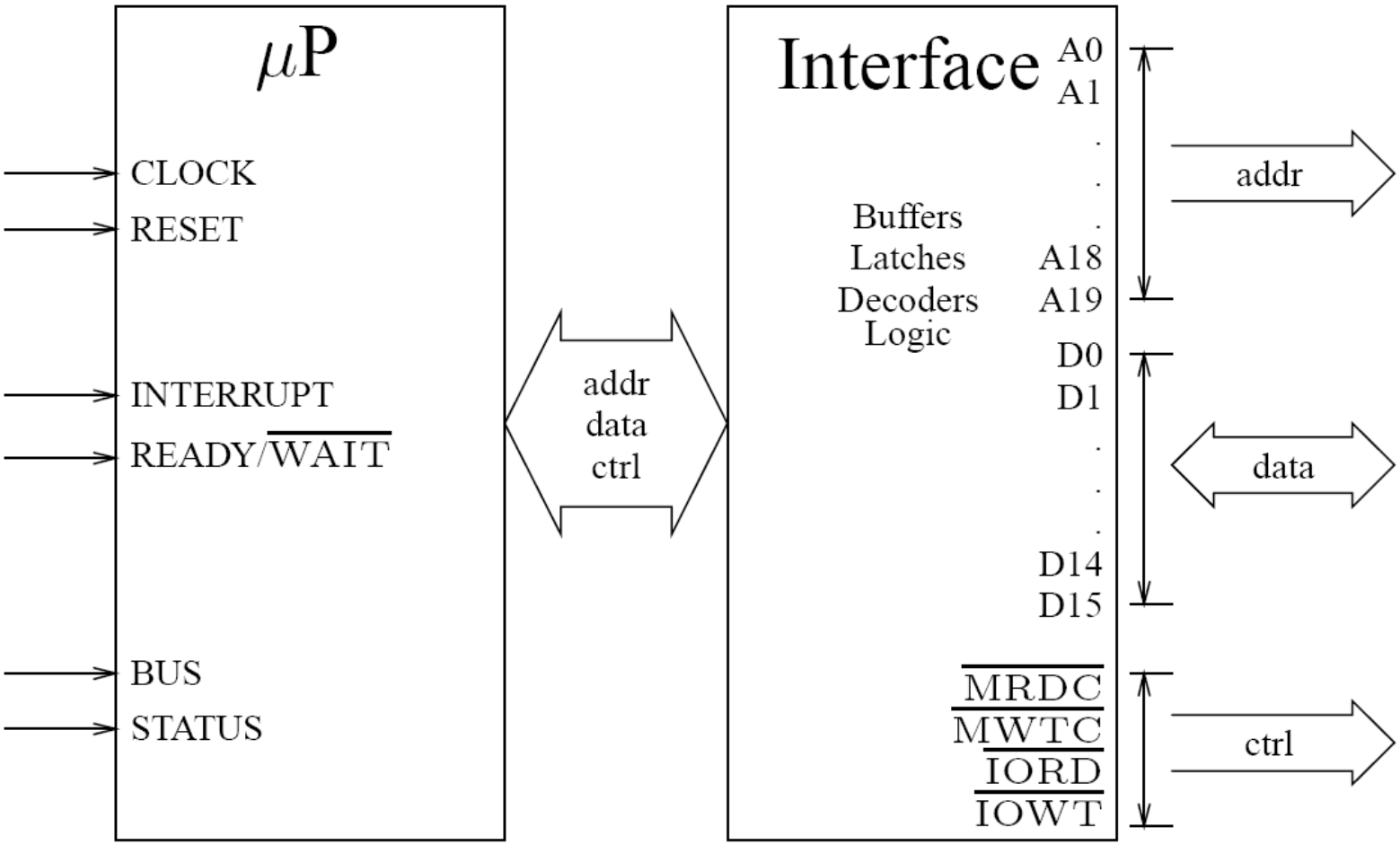
Topics/Reading

- Brey Chapter 9: Hardware specifications
  - Pin-outs & pin functions
  - 8274 Clock generator
  - Bus buffering & latching
  - Bus timing
  - Ready & the wait state
  - Minimum mode vs. maximum mode

8086/88 Hardware and Bus Structure

- We will now focus on the 8086/88 hardware and pin functions – later we will review characteristics of other Intel μP and the Motorola family.
- Although these μP's are fairly old, they still are a good way to introduce the Intel family of microprocessors.
- Both machines are 16-bit microprocessors. The 8088 has an 8-bit data bus and the 8086 has a 16-bit data bus.
- Still used in embedded systems (cost < $1)

8086/88 Hardware and Bus Structure



Abstract diagram showing data flow in/out of μP

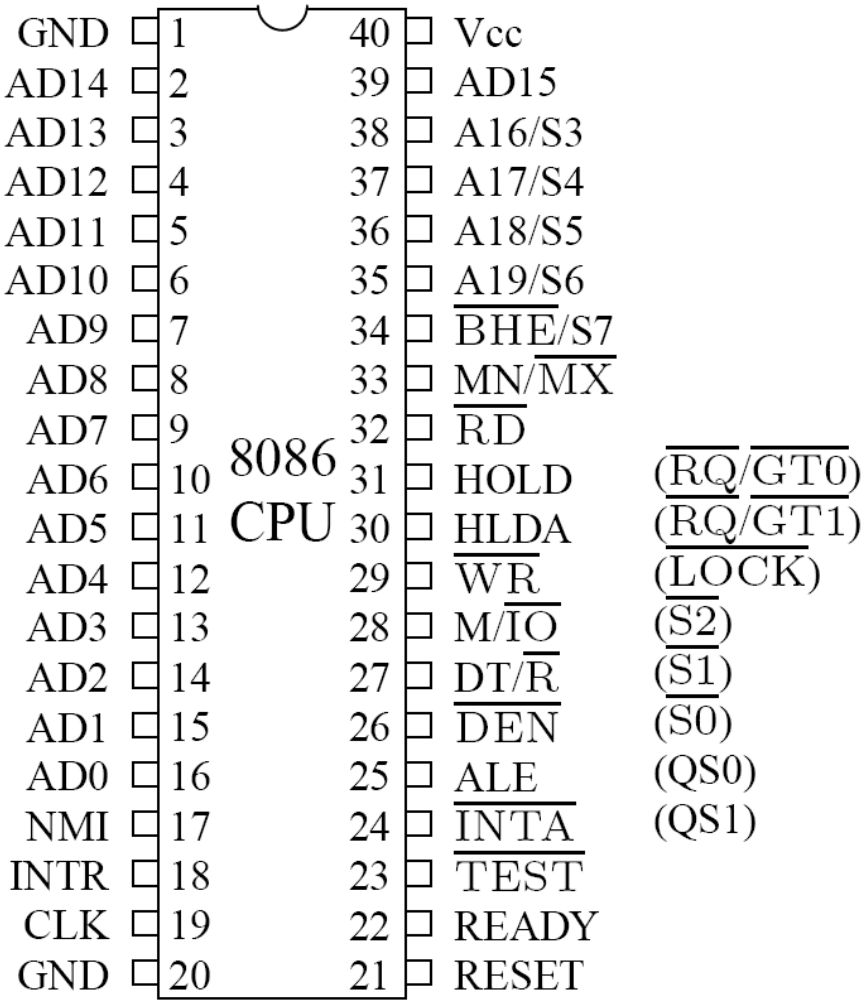
8086/88 Hardware and Bus Structure

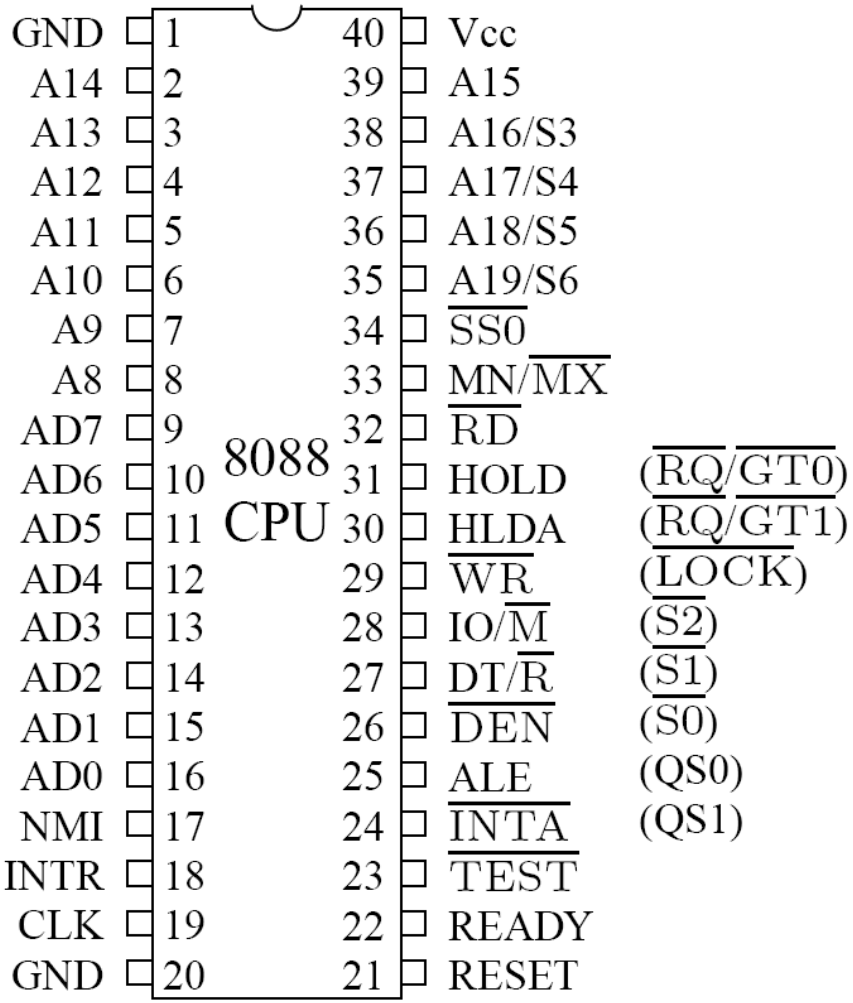
- **General Characteristics**
  - **Power:**
    - 8086 +5V ± 10%, 360mA (80C86 10mA)
    - 8088 +5V ± 10%, 340mA (80C86 10mA)
  - **Temp:**
    - 32ºF - 180ºF (not suitable for outdoors)
    - CMOS version -40ºF - 255ºF (MIL spec)
  - **Clock Frequency:**
    - normally 5MHz. SDK86: 2.5MHz or 5MHz.
  - **DC characteristics**
    - Must understand V-A characteristics of I/O pins in order to connect to the outside world. (next slide)

8086/88 Hardware and Bus Structure

- **Input characteristics**
  - compatible with standard logic-level components
    - logic 0: 0.8V max, 10μA max
    - logic 1: 2.0V min, 10μA max
  - The input current is very small – gates of MOSFETs, so current represents leakage.
- **Output characteristics**
  - logic 1 voltage level is compatible with most logic families, but logic 0 **is not**. (Most logic families have logic 0 max 0.4V)
    - logic 0: 0.45V max, ± 2.0 mA max
    - logic 1: 2.0V min, ± 400 μA max
  - No more than 10 loads per output without buffering.
  - If more than 10 loads are attached to any bus pin, then the entire 8086/8088 must be buffered.

8086/8088 Pin assignments & functions





8086/8088 DIP pin assignments (max mode in brackets)

8086/8088 Pin assignments & functions

- Both the 8086 and the 8088 are 40-pin Dual In-line Package (DIP) chips.
- 8086 – 16-bit μP and a 16-bit data bus
- 8088 – 16-bit μP and a 8-bit data bus
- 8086 has M/$\overline{IO}$, 8088 has IO/$\overline{M}$
  - See text Fig 9-1. Note that on 8088, $\overline{IO}$/M should be IO/$\overline{M}$
- Pin 34 is also different: 8086 $\overline{BHE}$/S7, 8088 has $\overline{SSO}$

8086/8088 Pin assignments & functions

- AD_{15} - AD_0
  - Multiplexed address/data bus.
  - lines carry address bits A_{15} - A_0 whenever ALE (Address Latch Enable) is logic 1.
  - lines carry data bits D_{15} - D_0 whenever ALE is logic 0.
  - Note: 8088 only multiplexes D_7 - D_0 because it uses an 8-bit data bus.
- A_{19}/S_6 - A_{16}/S_3
  - multiplexed address/status bits.
  - lines carry address bits A_{19} - A_{16} whenever ALE is logic 1.
  - lines carry status bits S_6 - S_3 whenever ALE is logic 0.

8086/8088 Pin assignments & functions

- S_6 always logic zero (not used).
- S_5 matches state of I flag bit (interrupt)
- S_4&S_3 reports segment being accessed during current bus cycle:

S_4	S_3	**Function**
0	0	Extra Segment (ES)
0	1	Stack Segment (SS)
1	0	Code Segment (CS)
1	1	Data Segment (DS)

- Note: These status lines could be decoded/latched to address four separate 1M banks of memory. (Split I/D)

8086/8088 Pin assignments & functions

- $\overline{RD}$ μP is set to receive data when low
- $\overline{WR}$ μP is outputting data when low
- M/$\overline{IO}$ (8086) indicates a memory address (‘1’), or an I/O address (‘0’).
- DT/$\overline{R}$ Data transmit/receive. Data bus is transmitting (‘1’), or receiving (‘0’) (for controlling bi-directional bus drivers).
- $\overline{DEN}$ Data bus enable – used to activate external buffers/transceivers.
- $\overline{BHE}$/S7 Bank high enable
  - used to enable D_{15} - D_8 in an 8086 during a 16-bit read/write.
  - Multiplexed with S7, which is not used (always 1).
  - latched with ALE.

8086/8088 Pin assignments & functions

- Pins to be discussed later:
  - *READY: Used to insert wait states (controlled by memory and IO for reads/writes) into the microprocessor.*
  - *RESET: Microprocessor resets if this pin is held high for 4 clock periods. Instruction execution begins at FFFF0H and IF flag is cleared.*
  - CLK: *Provides clock signal to 8086*
  - *HOLD: Requests a direct memory access (DMA). When 1, microprocessor stops and places address, data and control bus in high-impedance state.*
  - *HLDA (Hold Acknowledge): Indicates that the microprocessor has entered the hold state.*
  - RO/GT_1 *and* RO/GT_0: *Request/grant pins request/grant direct memory accesses (DMA) during maximum mode operation.*

8086/8088 Pin assignments & functions

- Pins to be discussed later:
  - *INTR: Used to request an interrupt*
  - *NMI: Used to request a non-maskable interrupt*
  - $\overline{\text{INTA}}$: *Output to acknowledge an interrupt.*
  - $\overline{\text{TEST}}$: *An input that is tested by the WAIT instruction. Commonly connected to the 8087 coprocessor.*
  - *QS_1 and QS_0: The queue status bits show status of internal instruction queue. Provided for access by the numeric coprocessor (8087).*
  - LOCK: *Lock output is used to lock peripherals off the system. Activated by using the LOCK: prefix on any instruction.*

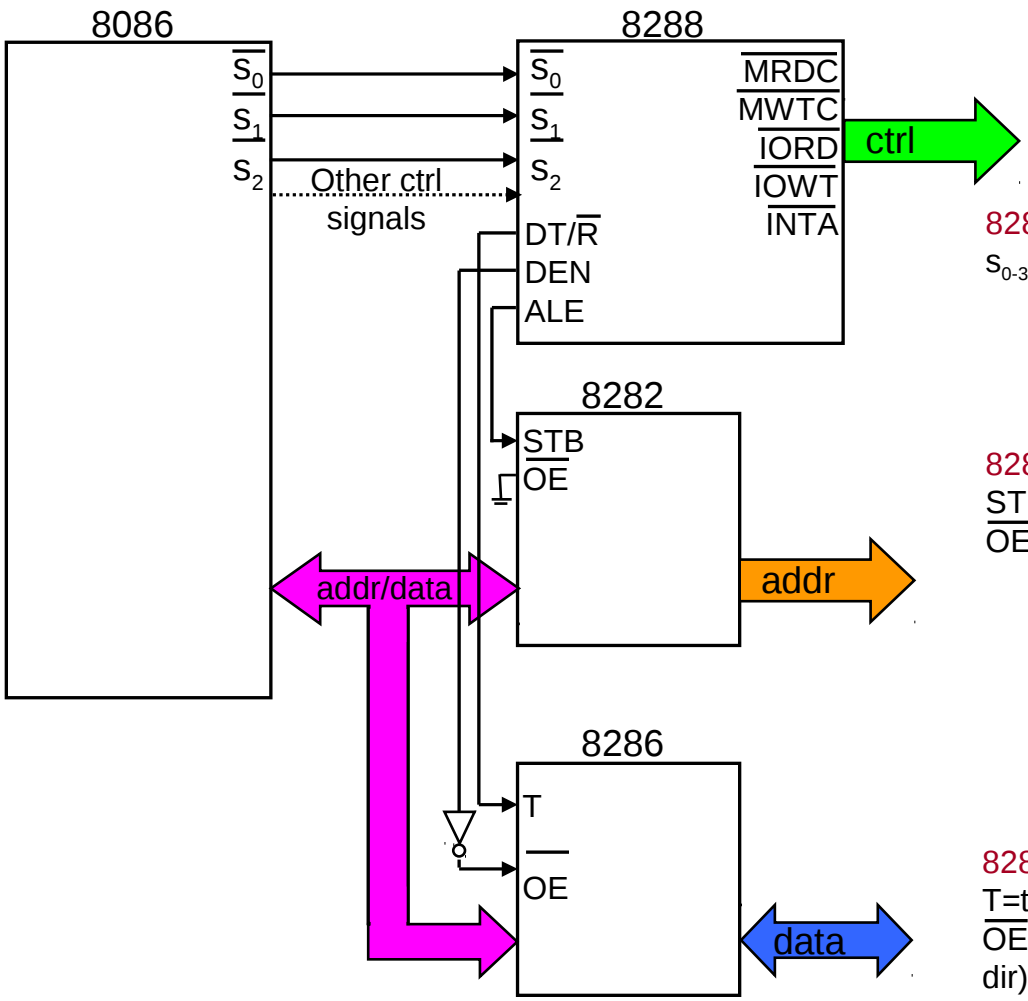
8086/8088 Pin assignments & functions

- Both the 8086 and the 8088 have two modes of operation:

  1. Minimum Mode: connect MN/$\overline{MX}$ to +5V (directly).
     - similar to 8085 operation.
     - all control signals for memory and I/O are generated by the μP.
     - ($\overline{RD}$, M/$\overline{IO}$, DT/$\overline{R}$, $\overline{DEN}$, ALE, $\overline{INTA}$, $\overline{WR}$, etc)

  2. Maximum Mode: connect MN/$\overline{MX}$ to ground (directly).
     - dropped by Intel beginning with the 80286.
     - must use with co-processor (8087) present.
     - some control signals must be generated externally.
     - use with 8288 bus controller.

8288 Bus Controller *(use when in MAX mode)*



8288 Bus Controller
$s_{0\text{-}3}$ = state data from 8086

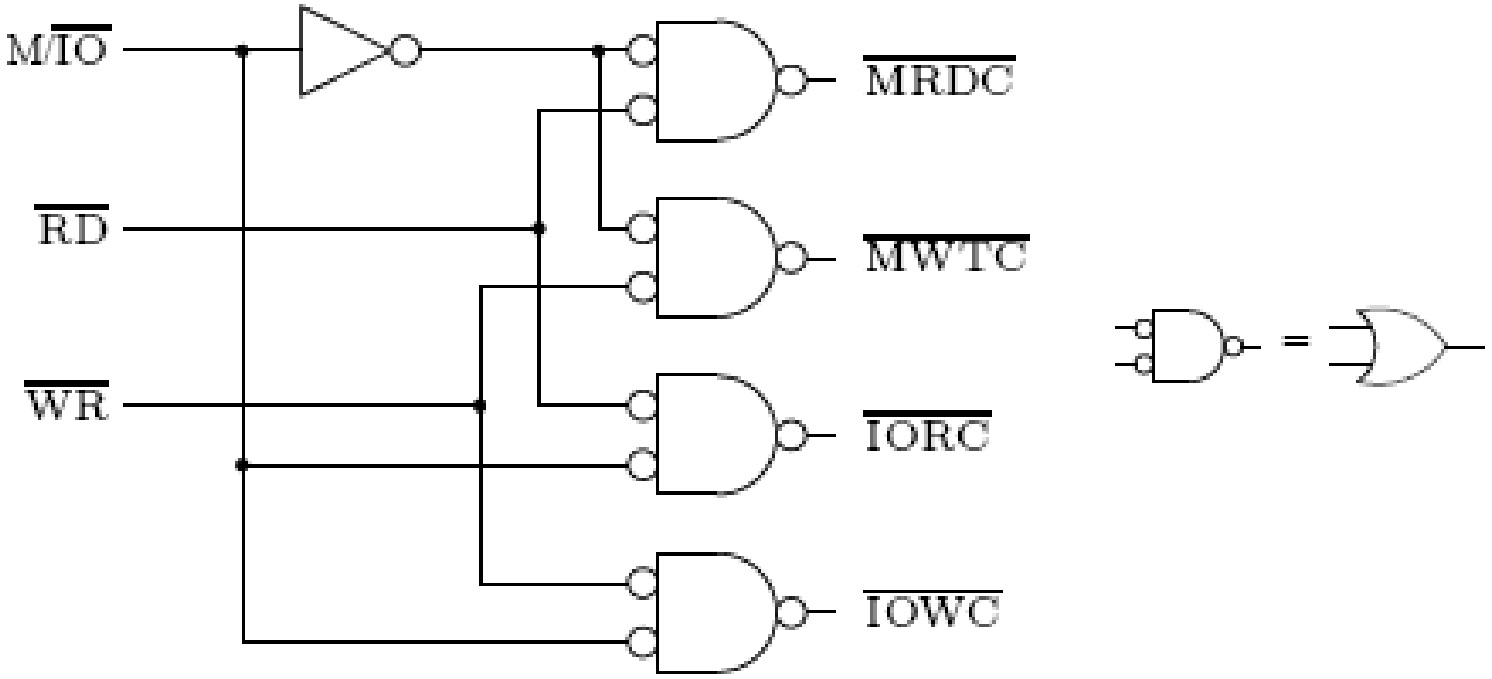
8282 Tri-State Octal Latch
STB=data strobe (admit new data)
$\overline{OE}$ = output enable

8286 Octal Bus Transceiver
T=transmit
$\overline{OE}$ = output enable (in either dir)

Some details omitted…
We will see how to achieve buffering & demultiplexing using generic chips…

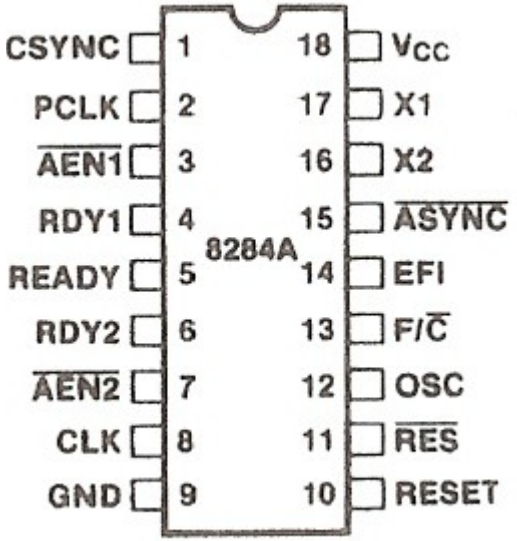
Decoding Bus Control Signal

- In *"max mode"* use 8288 bus controller to generate $\overline{\text{MRDC}}$,$\overline{\text{MWTC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$.
- In *"min mode"* (and for other processors) it is sometimes better to decode the available signals.



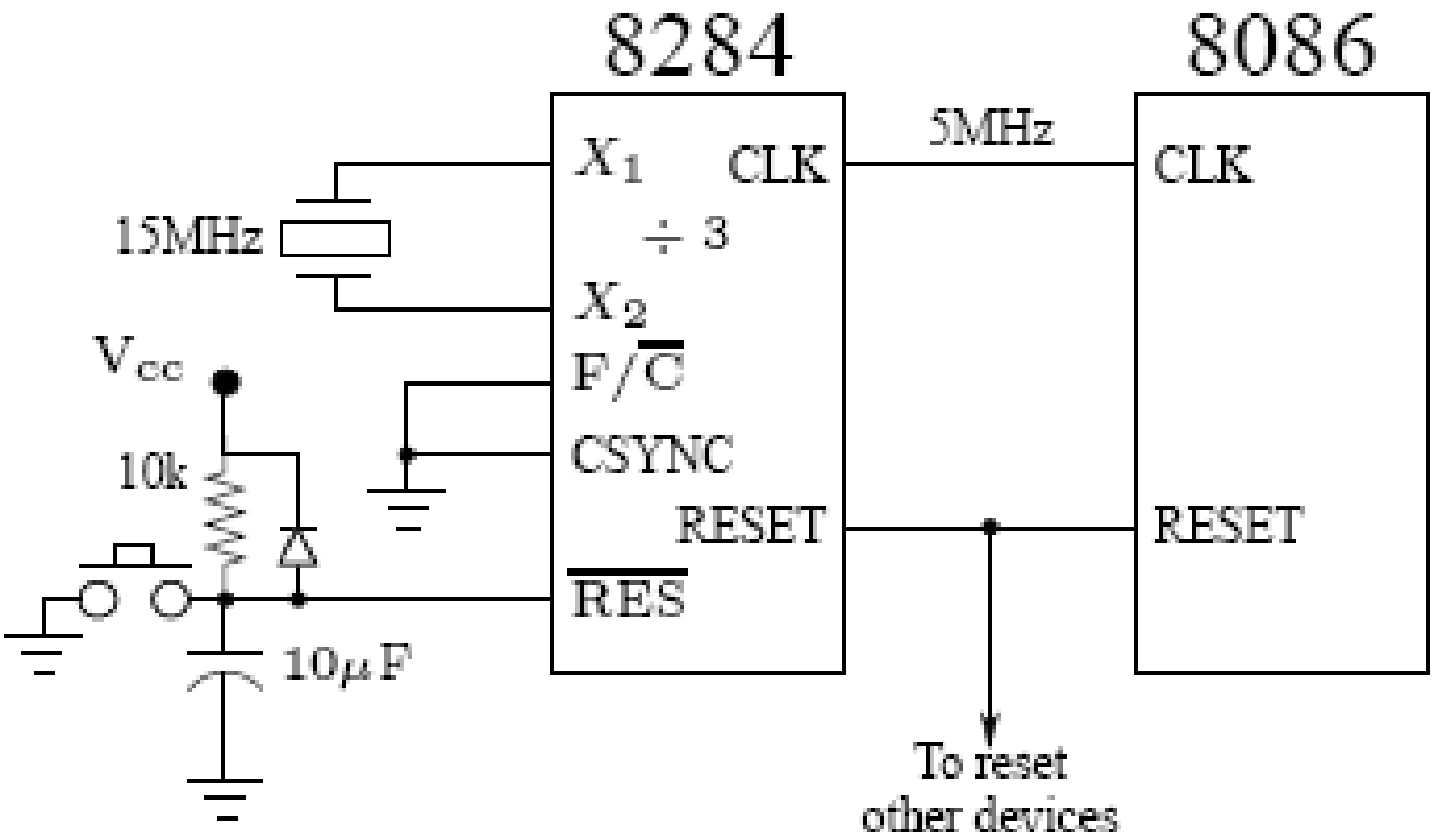
8284A Clock Generator

- Used with 8086/88 to generate
  1. clock signal (see next slide)
  2. reset signal (see next slide)
  3. ready signals (wait states)



- Inputs:
  - F/$\overline{C}$ Frequency/crystal select.
    1 → external clock
    0 → crystal (X1-X2 provides timing).
  - CSYNC Only used with external clock, otherwise grounded.
  - $\overline{RES}$ Reset input pin. Generates RESET output.

8284A Clock Generator



10K pullup? 0.5mA sink. (debouncing!)

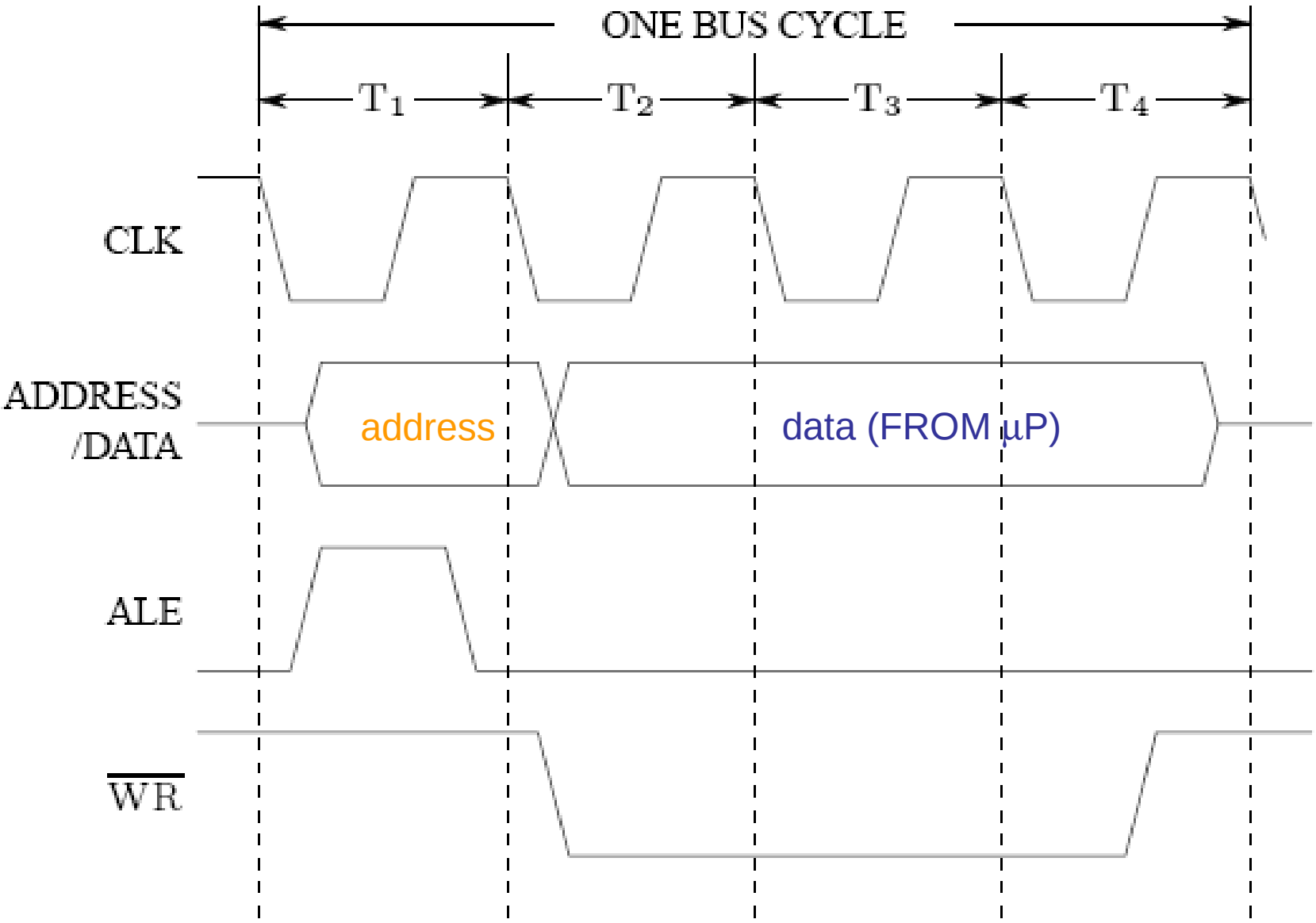
Bus Transfer Synchronization

- Synchronous busses (eg. Motorola 6800/11/12)
  - Transfer times and synchronization are tied to the system clock.
  - No facility for varying bus timing.
  - Clock generators could be used to vary bus speed (for slower memory), but would slow entire μP
- Semi-synchronous busses
  - provide for “wait states” to be inserted into bus timing (eg. 8086).
  - Allows more flexibility in interfacing to slower memory or I/O.
- Asynchronous busses (eg. Motorola 68000).
  - Requires extra bus signals for bus arbitration.
  - Requires *“acknowlegement”* signal from devices.
  - Requires bus time-out (watchdog).
  - Easier multiprocessor memory management.

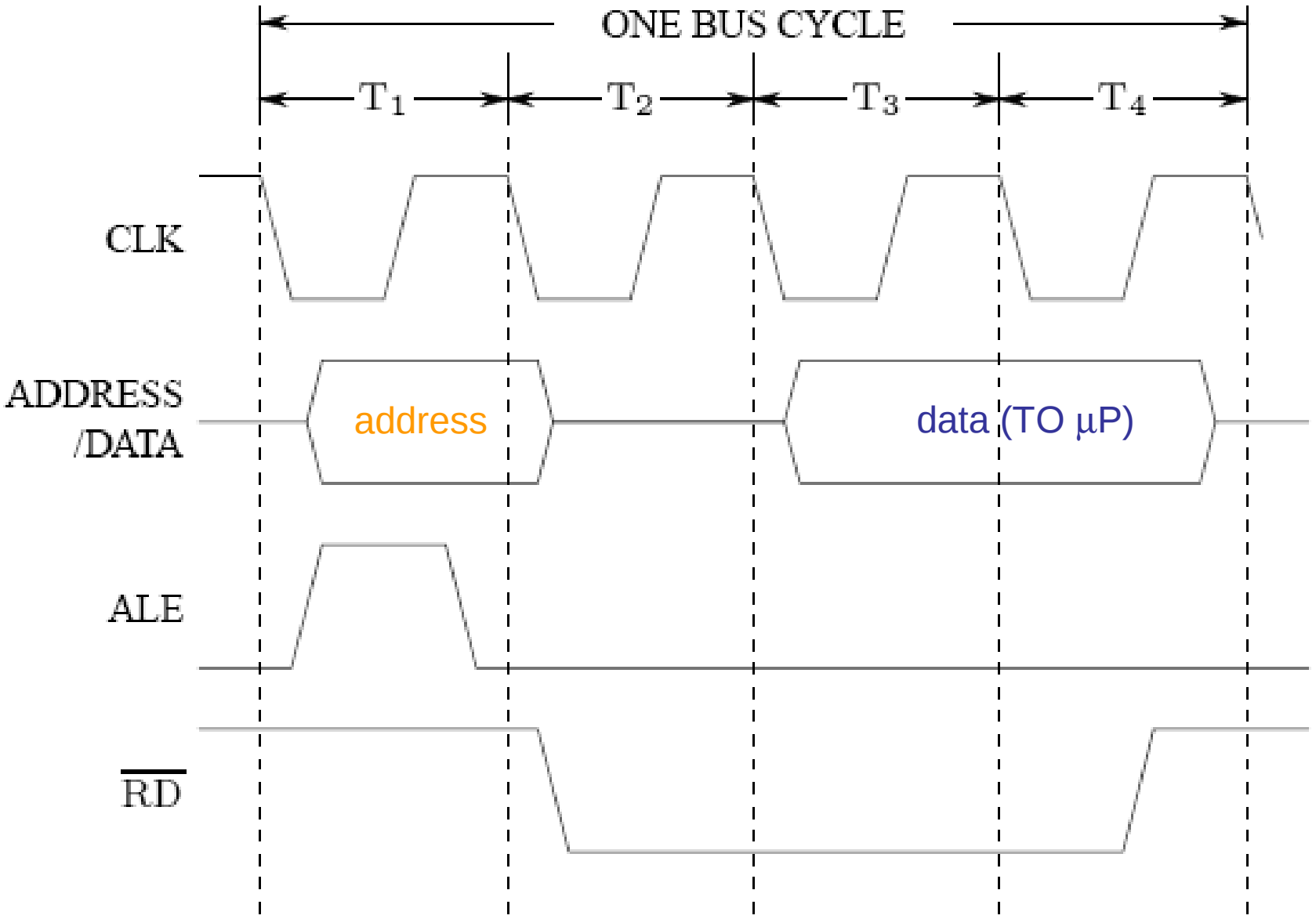
Bus Timing

- 8086 and 8088 bus cycles consume four system clock periods (T-states), T_1, T_2, T_3 and T_4.
- At 5MHz, each T-state is 200nS, therefore a bus cycle is 800nS.
- Semi-synchronous bus control allows inserting of wait states (T_w), also 200nS, between T_3 and T_4 which allows access to slow memory and I/O devices
  - (Text says T_w inserted between T_2 and T_3, but the Intel manual says between T_3 and T_4).
- Most processors are very similar in I/O and memory access operations.

Write Cycle


ONE BUS CYCLE
T1
T2
T3
T4
CLK
ADDRESS
/DATA
address
data (FROM µP)
ALE
WR

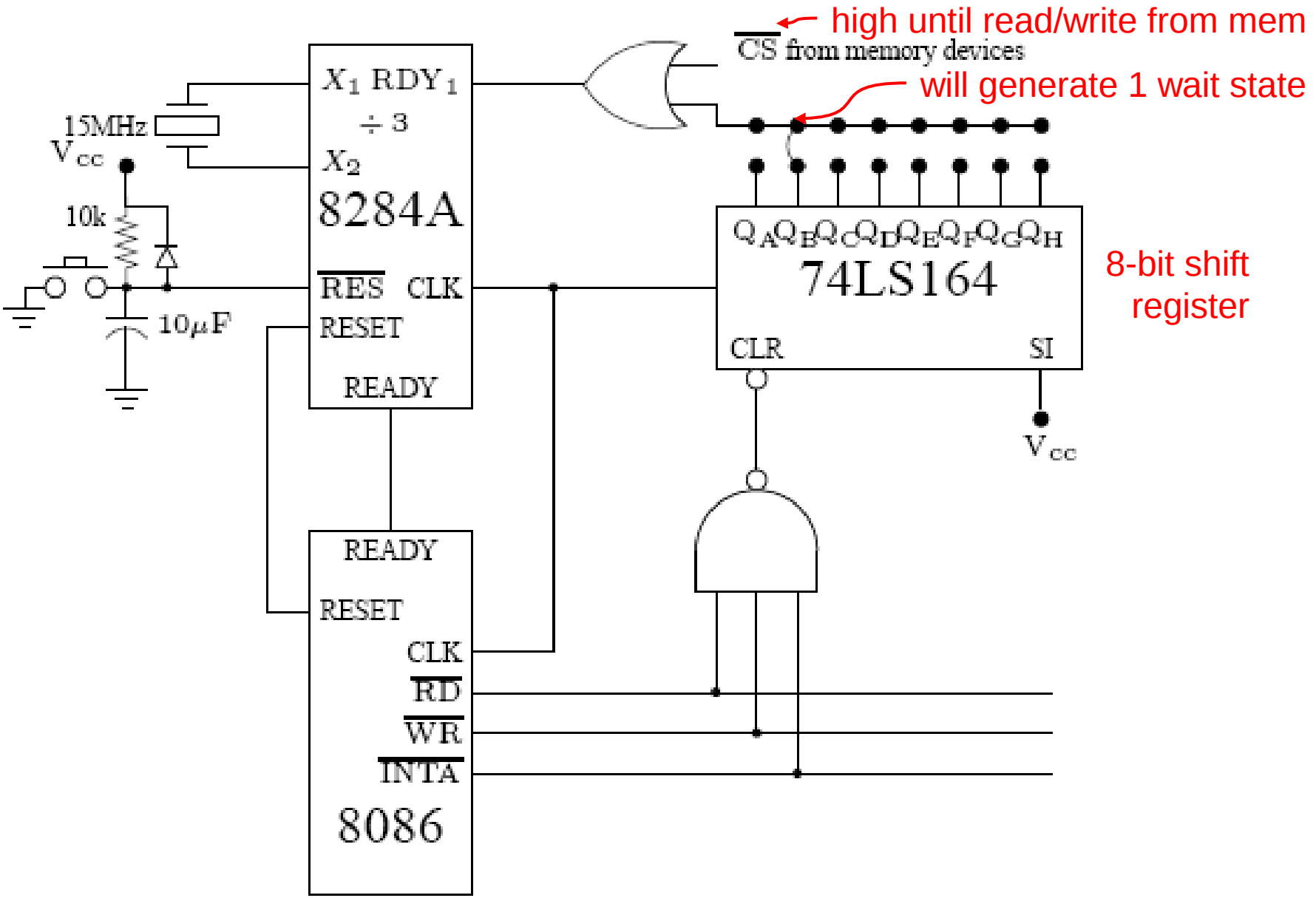
Read Cycle


ONE BUS CYCLE
T1
T2
T3
T4
CLK
ADDRESS
/DATA
address
data (TO µP)
ALE
RD

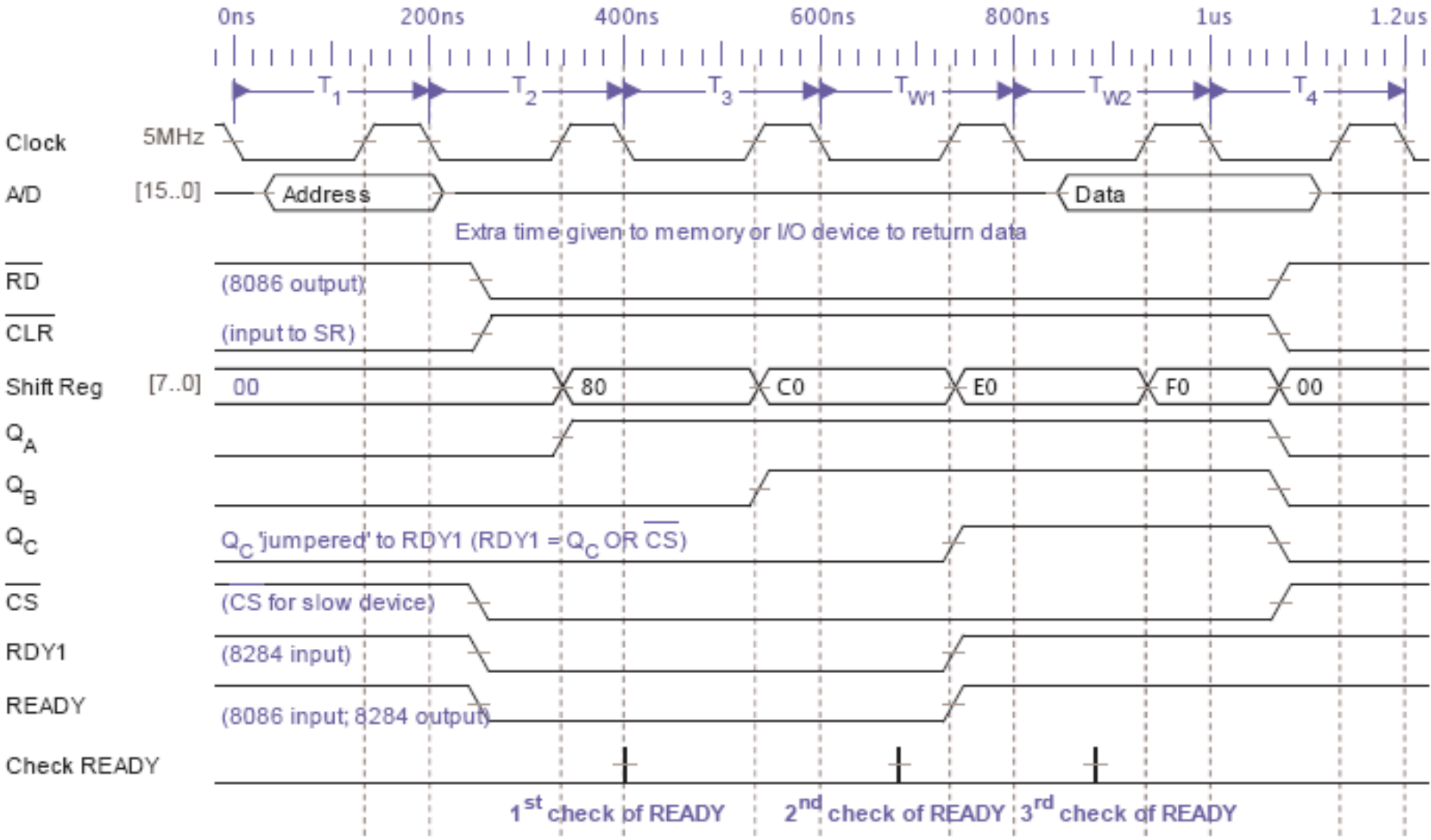
Read/Write Cycle Events

- T_1: Address, ALE, DT/R, $\overline{M}$/IO.
- T_2: $\overline{RD}$, $\overline{WR}$, $\overline{DEN}$, data on the bus (for write).
- At the end of T_2 (middle of T_3), μP samples READY.
  - (a) while READY = 0; do
  - (b) insert T_w.
- T_3/T_w: Gives time for memory or I/O device to read/write.
- For read cycles, data bus is sampled at end of T_3.
- T_4: All bus signals are deactivated.
- Normal memory access time is 460nS. Slower devices will need at least one wait state which will give 660nS.

Wait State Generation using 8284A

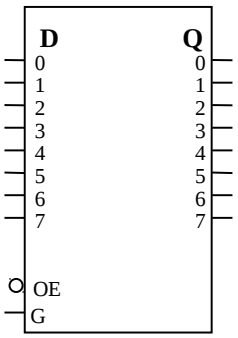


Example Timing for 2 Wait States

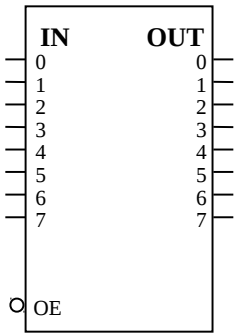


Bus Latching and Buffering

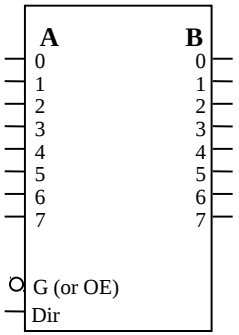
- Latches are used to de-multiplex the address/data and address/status lines and commonly have output buffers for driving external loads.
- Buffers are used to drive external loads, and to isolate component when disabled.



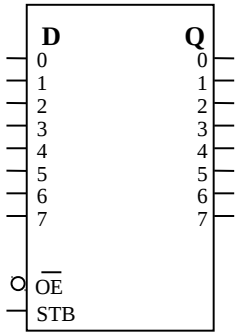
74LS373
Octal Latch



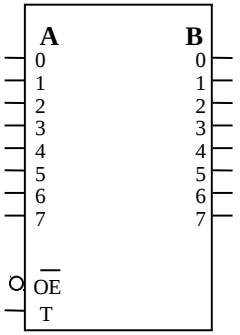
74LS244
Octal 3-State Buffer



74LS245
Bus Transceiver

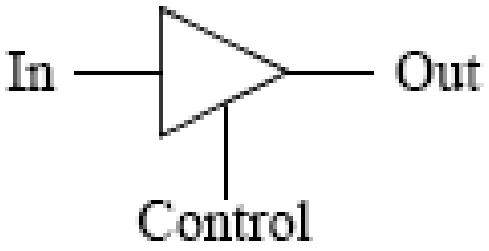


8282
Tri-state Octal Latch



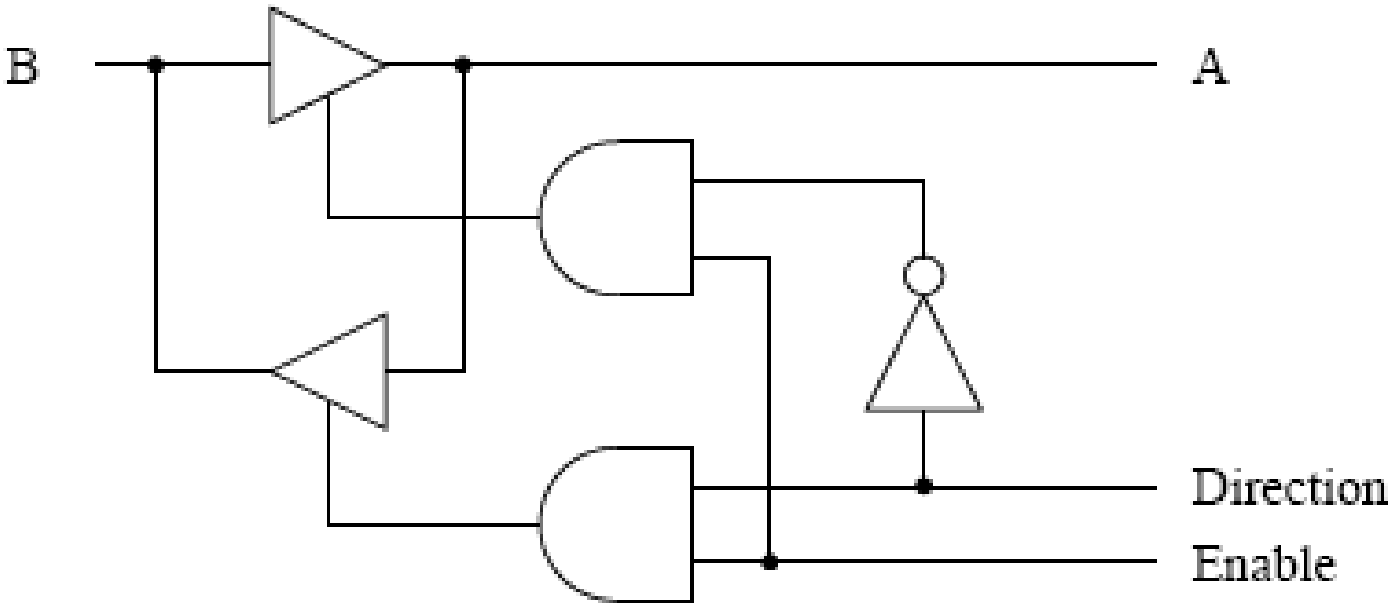
8286
Tri-state Octal Bus Transceiver

Three-state Buffer (Tri-state buffer)



- When enabled by the control line, output follows input (buffered, pass-through).
- When disabled, output is a very high impedance which prevents the output from driving or loading connected circuits.
- When disabled, the outputs are said to be floating.
- In effect, it is like a switch.

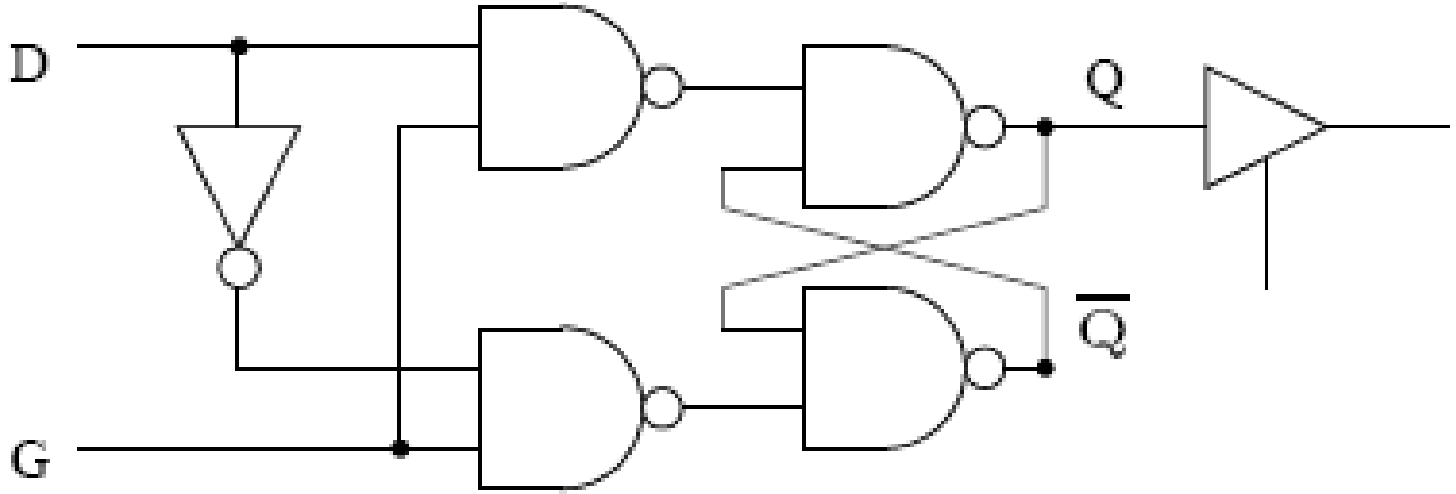
Bidirectional buffers (transceivers)



DIR	Action
0	$B \rightarrow A$
1	$A \rightarrow B$

EX: 74LS245 octal bus transceiver.

Latches (D-type flip-flops)



- When enable is high, Q follows D.
- When enable goes low, Q maintains (latches) state of D.
- Eg:
  - 74LS373 (latched on falling edge).
  - 74LS374 (latched on rising edge)

A fully buffered 8086